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				APPLICANT: Peter BALLAM	
Sheet	1	of	1	GROUP ART UNIT: 2125	EXAMINER: Albert William Paladini

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
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FOREIGN PATENT DOCUMENTS

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OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
A W P		JOANNE E. DEGROAT, Transparent Logic Modeling in VHDL, IEEE Design & Test of Computers, US, IEEE Computers Society, Los Alamitos, vol. 7, no. 3, June 1, 1990, pages 42-48, XP000205089	

EXAMINER ALBERT W. PALADINI PATENT EXAMINER	<i>Albert W. Paladini</i>	DATE CONSIDERED 4-13-05
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#EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. ___, filed ___, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

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